TS64MMD64V6F

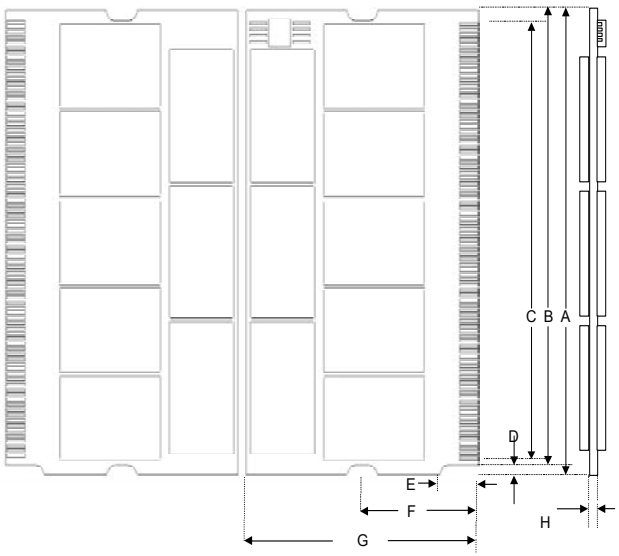
512MB 172 PIN PC266 DDR MICRO-DIMM With 32Mx8 2.5VOLT

Description

The TS64MMD64V6F is a 64M x 64bits Double Data Rate SDRAM high density for DDR266. The TS64MMD64V6F consists of 16pcs CMOS 32Mx8 bits Double Data Rate SDRAMs in 60 Ball SOC/TFBGA packages and a 2048 bits serial EEPROM on a 172-pin printed circuit board. The TS64MMD64V6F is a Dual In-Line Memory Module and is intended for mounting into 172-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Placement



PCB : 09-1910

Features

- Power supply: VDD= VDDQ: 2.5V ± 0.2V
- Max clock Freq: 133MHZ.
- Double-data-rate architecture; two data transfers per clock cycle
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CLK transition
- Commands entered on each positive CLK edge
- Auto and Self Refresh.
- Data I/O transactions on both edge of data strobe.
- Serial Presence Detect (SPD) with serial EEPROM
- SSTL-2 compatible inputs and outputs.
- MRS cycle with address key programs.
  - CAS Latency (Access from column address): 2.5
  - Burst Length (2,4,8)
  - Data Sequence (Sequential & Interleave)

Dimensions

Side	Millimeters	Inches
A	45.50 ± 0.20	1.791 ± 0.008
B	44.50	1.752
C	42.50	1.673
D	1.00	0.039
E	5.00	0.197
F	15.00	0.591
G	30.00± 0.20	1.181± 0.008
H	0.80 ± 0.10	0.031 ± 0.004

(Refer Placement)

Pin Identification

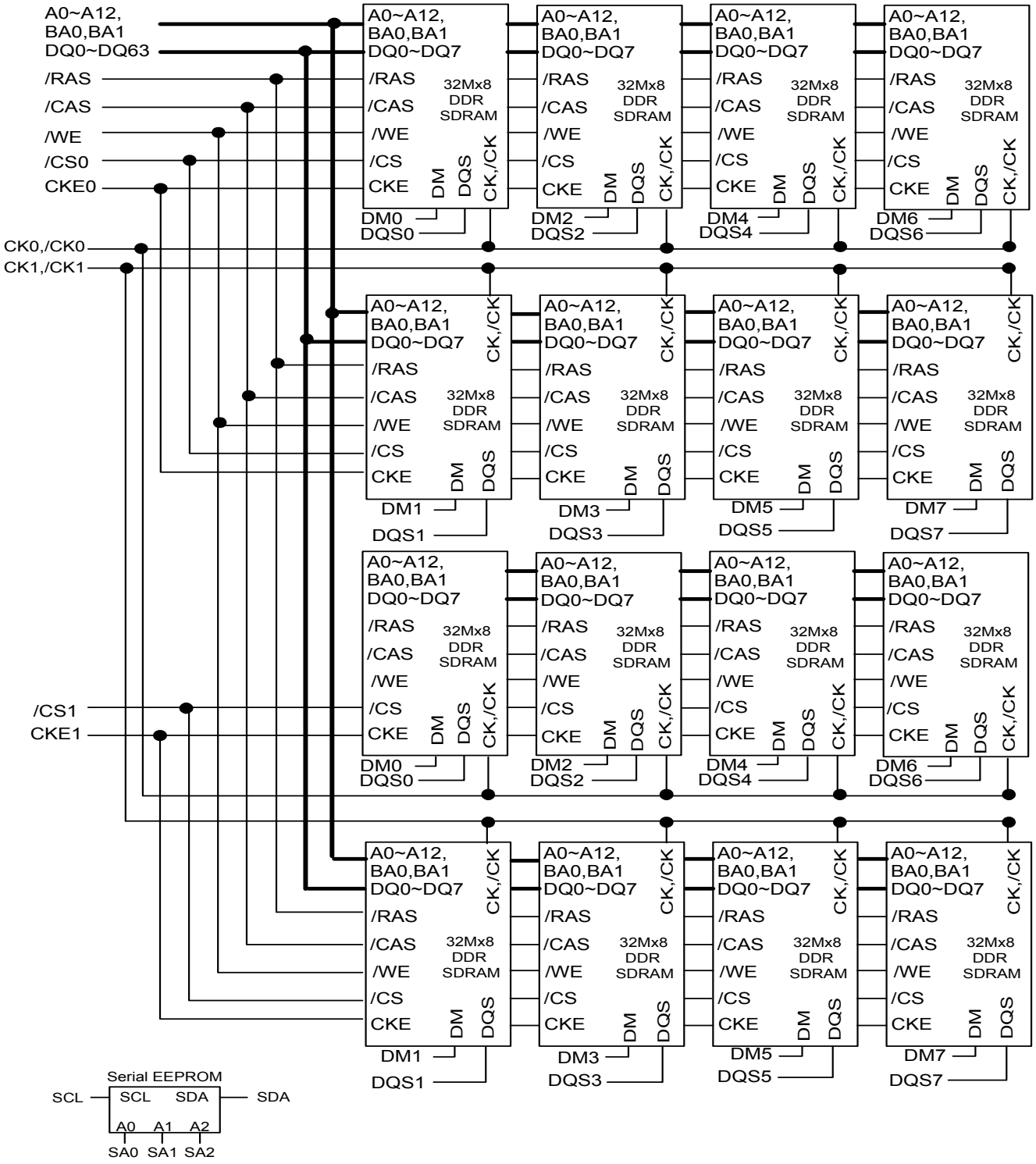
Symbol	Function
A0~A12, BA0,BA1	Address input
DQ0~DQ63	Data Input / Output.
DQS0~DQS7	Data strobe input/output
CK0~CK1 /CK0~CK1	Clock Input.
CKE0,CKE1	Clock Enable Input.
/CS0,/CS1	Chip Select Input.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DM0~DM7	Data-in Mask
VDD	+2.5 Voltage power supply
VDDQ	+2.5 Voltage Power Supply for DQS
VREF	Power Supply for Reference
VDDSPD	+2.5 Voltage Serial EEPROM Power Supply
SA0~SA2	Address in EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
VSS	Ground
NC	No Connection

(Refer Block Diagram AND Pinouts)

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	V_{REF}	59	DQ25	117	V_{DD}	02	V_{REF}	60	DQ29	118	V_{DD}
03	Vss	61	DQS3	119	DQ41	04	Vss	62	DM3	120	DQ45
05	DQ0	63	Vss	121	DQS5	06	DQ4	64	Vss	122	DM5
07	DQ1	65	DQ26	123	Vss	08	DQ5	66	DQ30	124	Vss
09	V_{DD}	67	DQ27	125	DQ42	10	V_{DD}	68	DQ31	126	DQ46
11	DQS0	69	V_{DD}	127	DQ43	12	DM0	70	V_{DD}	128	DQ47
13	DQ2	71	CKE1	129	V_{DD}	14	DQ6	72	CKE0	130	V_{DD}
15	Vss	73	A12	131	V_{DD}	16	Vss	74	A11	132	/CK1
17	DQ3	75	A9	133	Vss	18	DQ7	76	A8	134	CK1
19	DQ8	77	A7	135	Vss	20	DQ12	78	A6	136	Vss
21	V_{DD}	79	Vss	137	DQ48	22	V_{DD}	80	Vss	138	DQ52
23	DQ9	81	A5	139	DQ49	24	DQ13	82	A4	140	DQ53
25	DQS1	83	A3	141	V_{DD}	26	DM1	84	A2	142	V_{DD}
27	Vss	85	A1	143	DQS6	28	Vss	86	A0	144	DM6
29	DQ10	87	A10/AP	145	DQ50	30	DQ14	88	BA1	146	DQ54
31	DQ11	89	V_{DD}	147	Vss	32	DQ15	90	V_{DD}	148	Vss
33	V_{DD}	91	BA0	149	DQ51	34	V_{DD}	92	/RAS	150	DQ55
35	CLK0	93	/WE	151	DQ56	36	V_{DD}	94	/CAS	152	DQ60
37	/CLK0	95	/CS0	153	V_{DD}	38	Vss	96	/CS1	154	V_{DD}
39	Vss	97	NC	155	DQ57	40	Vss	98	NC	156	DQ61
41	DQ16	99	Vss	157	DQS7	42	DQ20	100	Vss	158	DM7
43	DQ17	101	DQ32	159	Vss	44	DQ21	102	DQ36	160	Vss
45	V_{DD}	103	DQ33	161	DQ58	46	V_{DD}	104	DQ37	162	DQ62
47	DQS2	105	V_{DD}	163	DQ59	48	DM2	106	V_{DD}	164	DQ63
49	DQ18	107	DQS4	165	V_{DD}	50	DQ22	108	DM4	166	V_{DD}
51	Vss	109	DQ34	167	SDA	52	Vss	110	DQ38	168	SA0
53	DQ19	111	Vss	169	SCL	54	DQ23	112	Vss	170	SA1
55	DQ24	113	DQ35	171	V_{DD}SPD	56	DQ28	114	DQ39	172	SA2
57	V_{DD}	115	DQ40			58	V_{DD}	116	DQ44		

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on V_{DD} supply to Vss	VDD, VDDQ	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55~+150	°C
Power dissipation	P_D	9.5	W
Short circuit current	I_{OS}	50	mA
Mean time between failure	MTBF	50	Years
Temperature Humidity Burning	THB	85°C/85%, Static Stress	°C-%
Temperature Cycling Test	TC	0°C ~ 125°C Cycling	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	VDD	2.3	2.7	V	
I/O Supply voltage	VDDQ	2.3	2.7	V	
I/O Reference voltage	VREF	V_{DDQ}/2-50mV	V_{DDQ}/2+50mV	V	1
I/O Termination voltage	VTT	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	VIH(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	4
Input logic low voltage	VIL(DC)	-0.3	V_{REF}-0.15	V	4
Input Voltage Level, CK and /CK inputs	VIN(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and /CK inputs	VID(DC)	0.3	V_{DDQ}+0.6	V	3
Input crossing point voltage, CK and /CK inputs	VIX(DC)	1.15	1.35	V	5
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current (Normal strength driver) VOUT= VTT + 0.84V	I_{OH}	-16.8		mA	
Output Low Current (Normal strength driver) VOUT= VTT – 0.84V	I_{OL}	16.8		mA	
Output High Current(Half strength driver) VOUT= VTT + 0.45V	I_{OH}	-9		mA	
Output High Current(Half strength driver) VOUT= VTT - 0.45V	I_{OL}	9		mA	

Note:
1. Includes ± 25mV margin for DC offset on VREF, and a combined total of ± 50mV margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled. TO VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of <=3nH.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
5. The value of V_{IX} is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted,VDD=2.7V TA = 10°C)

Parameter	Symbol	Max.	Unit	Note
Operating current - One bank Active-Precharge; tRC=tRCmin; tCK= tCK min DQ, DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle	IDD0	800	mA	
Operating current - One bank Active-Read-Precharge; Burst=2; tRC=tRC min; CL=2.5; tCK=tCK min; VIN=VREF fro DQ,DQS and DM	IDD1	960	mA	
Precharge power-down standby current; All banks idle; power –down mode; CKE = <VIL(max); tCK= tCK min VIN = VREF for DQ, DQS and DM	IDD2P	120	mA	
Precharge Floating standby current; CS# > =VIH(min);All banks idle; CKE > = VIH(min); tCK=133Mhz for DDR266 Address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS and DM	IDD2F	500	mA	
Active power - down standby current; one bank active; power-down mode; CKE<= VIL (max); tCK = tCK min; VIN = VREF for DQ, DQS and DM	IDD3P	500	mA	
Active standby current; CS# >= VIH(min); CKE>=VIH(min); one bank active; active - precharge; tRC=tRASmax; tCK = tCK min; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N	740	mA	
Operating current - burst read; Burst length = 2; reads; continguous burst; One bank active; address and control inputs changing once per clock cycle; CL=2.5 at tCK = tCK min ; 50% of data changing at every burst; lout = 0 mA	IDD4R	1520	mA	
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; CL=2.5 at tCK = tCK min ; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	IDD4W	1360	mA	
Auto refresh current; tRC = tRFC(min)	IDD5	1520	mA	
Self refresh current; CKE <= 0.2V;	IDD6	48	mA	
Operating current - Four bank operation; Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	IDD7	2400	mA	

Note: 1. Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading capacitor.

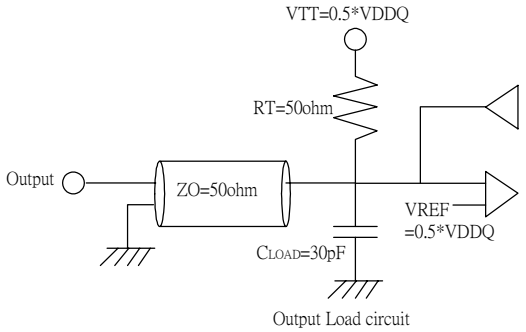
AC OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ + 0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ - 0.2	0.5*VDDQ + 0.2	V	2

Note:
1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS (VDD=2.5, VDDQ=2.5, TA=0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5*VDDQ	V	
Input signal maximum peak swing	1.5	V	
Input Levels(VIH/VIL)	VREF+0.31/VREF-0.31	V	
Input timing measurement reference level	VREF	V	
Output timing measurement reference level	VTT	V	
Output load condition	See Load Circuit		



Output Load circuit

Input/Output CAPACITANCE (VDD = 2.5V, VDDQ = 2.5V,TA = 25°C, f = 1MHz)

	Symbol	Min		Unit
Input capacitance (A0~A12, BA0~BA1, /RAS, /CAS, /WE)	CIN1	36	45	pF
Input capacitance (CKE0)	CIN2	36	45	pF
Input capacitance (/CS0)	CIN3	34	42	pF
Input capacitance (CK0, CK1)	CIN4	34	38	pF
Input capacitance (DM0~DM8)	CIN5	8	9	pF
Data and DQS input/output capacitance (DQ0~DQ63)	COUT1	8	9	pF

AC Timing Parameters & Specifications

(These AC characteristics were tested on the Component)

Parameter	Symbol	Min	Max	Unit	Note
Row cycle time	tRC	65		ns	
Refresh row cycle time	tRFC	75		ns	
Row active time	tRAS	45	120K	ns	
/RAS to /CAS delay	tRCD	20		ns	
Row active to Row active delay	tRP	20		ns	
Row active to Row active delay	tRRD	15		ns	
Write recovery time	tWR	15		ns	
Last data in to Read command	tWTR	1		tCK	
Col. Address to Col. Address delay	tCCD	1		tCK	
Clock cycle time	tCK	7.5		ns	4
Clock high level width	tCH	0.45	0.55	tCK	
Clock low level width	tCL	0.45	0.55	tCK	
DQS-out access time from CK /CK	tDQSCK	-0.75	0.75	ns	
Output data access time from CK /CK	tAC	-0.75	0.75	ns	
Data strobe edge to output data edge	tDQSQ	-	0.5	ns	4
Read Preamble	tRPRE	0.9	1.1	tCK	
Read Postamble	tRPST	0.4	0.6	tCK	
CK to valid DQS-in	tDQSS	0.75	1.25	tCK	
DQS-in setup time	tWPRES	0		ns	2
DQS-in hold time	tWPREH	0.25		tCK	
DQS falling edge to CK rising-setup time	tDSS	0.2		tCK	
DQS falling edge from CK rising-hold time	tDSH	0.2		tCK	
DQS-in high level width	tDQSH	0.35		tCK	
DQS-in low level width	tDQSL	0.35		tCK	
DQS-in cycle time	tDSC	0.9	1.1	tCK	
Address and Control input setup time	tIS	0.9		ns	
Address and Control input hold time	tIH	0.9		ns	
Data-out high-impedance time from CK, /CK	tHZ	-0.75	0.75	ns	
Data-out low-impedance time from CK, /CK	tLZ	-0.75	0.75	ns	
Mode register set cycle time	tMRD	15		ns	
DQ & DM setup time to DQS	tDS	0.5		ns	

DQ & DM hold time to DQS	tDH	0.5		ns	
DQ & DM input pulse width	tDIPW	1.75		ns	
Power down exit time	tPDEX	7.5		ns	
Exit self refresh to bank active command	tXSA	75		ns	5
Exit self refresh to read command	tXSR	200		Cycle	
Refresh interval time	tREF	7.8		us	1
Clock half period	tHP	tCLmin or tCHmin		ns	
Data hold skew factor	tQHS		0.75	ns	
DQS write postamble time	tWPST	0.4	0.6	TCK	3

Note:
1. Maximum burst refresh of 8
2. The specific requirement is that DQS be valid (High or Low) on or before this CK edge. The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The Maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. For registered DIMMs, tCL and tCH are >= 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.
5. A write command can be applied with tRCD satisfied after this command.

SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	$BA_{0,1}$	A_{10}/AP	A_0~A_9, A_{11}, A_{12}	Note
Register	Extended Mode Register Set		H	X	L	L	L	L	OP CODE			1,2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down	Entry		H	L	H	X	X	X	X			
					L	V	V	V				
	Exit		L	H	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X			
					L	H	H	H				
	Exit		L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No Operation Command			H	X	H	X	X	X	X			9
					L	H	H	H				9

Note:
1. OP Code: Operand Code. A0 ~ A12 & BA0 ~ BA1: Program keys. (@EMRS/MRS)
2. EMRS/ MRS can be issued only at all banks precharge state. A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM. The automatically precharge without row precharge command is meant by "Auto". Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1: Bank select addresses. If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected. If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected. If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected. If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command cannot be issued. Another bank read/write command can be issued after the end of burst. New row active of the associated bank can be issued at tRP after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in is masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation (NOP)" in DDR SDRAM.

Serial Presence Detect Specification

Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	# of Bytes Written into Serial Memory	128bytes	80
1	Total # of Bytes of S.P.D Memory	256bytes	08
2	Fundamental Memory Type	DDR SDRAM	07
3	# of Row Addresses on this Assembly	13	0D
4	# of Column Addresses on this Assembly	10	0A
5	# of Module Rows on this Assembly	2 bank	02
6	Data Width of this Assembly	64bits	40
7	Data Width of this Assembly	0	00
8	VDDQ and Interface Standard of this Assembly	SSTL 2.5V	04
9	DDR SDRAM Cycle Time at CAS Latency=2.5	7.5ns	75
10	DDR SDRAM Access Time from Clock at CL=2.5	± 0.75ns	75
11	DIMM configuration type (non-parity, Parity, ECC)	NON-ECC	00
12	Refresh Rate Type	7.8us/Self Refresh	82
13	Primary DDR SDRAM Width	X8	08
14	Error Checking DDR SDRAM Width	-	00
15	Min Clock Delay for Back to Back Random Column Address	tCCD=1CLK	01
16	Burst Lengths Supported	2,4,8	0E
17	# of banks on each DDR SDRAM device	4 bank	04
18	CAS Latency supported	2, 2.5	0C
19	CS Latency	0 CLK	01
20	WE Latency	1 CLK	02
21	DDR SDRAM Module Attributes	Registered address & control inputs and on-card DLL	20
22	DDR SDRAM Device Attributes: General	+/-0.2V voltage tolerance	00
23	DDR SDRAM Cycle Time CL=2.0	10ns	A0
24	DDR SDRAM Access from Clock CL=2.0	± 0.75ns	75
25	DDR SDRAM Cycle Time CL=1.5	-	00
26	DDR SDRAM Access from Clock CL=1.5	-	00
27	Minimum Row Precharge Time (tRP)	20ns	50
28	Minimum Row Active to Row Activate delay (tRRD)	15ns	3C
29	Minimum RAS to CAS Delay (tRCD)	20ns	50
30	Minimum active to Precharge time (tRAS)	45ns	2D
31	Module ROW density	256MB	40
32	Command/Address Input Setup Time	0.9ns	90
33	Command/Address Input Hold Time	0.9ns	90
34	Data Signal Input Setup Time	0.5ns	50
35	Data Signal Input Hold Time	0.5ns	50
36-61	Superset Information	-	00
62	SPD Data Revision Code	-	00
63	Checksum for Bytes 0-62	-	C0

64-71	Manufacturers JEDEC ID	Transcend	7F, 4F					
72	Manufacturing Location	T	54					
73-90	Manufacturers Part Number	TS64MMD64V6F	54	53	36	34	4D	4D
			44	36	34	56	36	46
			20	20	20	20	20	20
91-92	Revision Code	-	-					
93-94	Manufacturing Date	By Manufacturer	Variable					
95-98	Assembly Serial Number	By Manufacturer	Variable					
99-127	Manufacturer Specific Data	-	-					
128~255	Unused Storage Locations	Undefined	-					